(15) Please cancel Claim 15 without prejudice or disclaimer.

## REMARKS/ARGUMENTS

The Applicants respectfully request reconsideration of this Application. The Applicants originally submitted Claims 1-15 in the Application. The Applicants have amended Claims 1-8 and 10-14 and have canceled Claims 9 and 15. No claims have been added. Accordingly, Claims 1-8 and 10-14 are currently pending in the Application.

### I. Formal Matters and Objections

In response to a restriction requirement by the Examiner, the Applicants hereby formally agree to prosecute Group I, Claims 1-8 and 10-14. As a result, Claims 9 and 15 have been canceled without prejudice or disclaimer pending the filing of Divisional Applications.

### II. Rejection of Claims 12 and 14 under 35 U.S.C. §112

The Examiner has rejected Claims 12 and 14 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. In response, the Applicants have amended Claims 12 and 14 to fully comply with the requirements of §112, second paragraph. Accordingly, the Applicants respectfully request the Examiner withdraw the §112, second paragraph, rejection with respect to Claims 12 and 14.

## III. Rejection of Claims 1, 2, 4-8, 10-12 and 14 under 35 U.S.C. §102

The Examiner has rejected Claims 1, 2, 4-8, 10-12 and 14 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,201,308 to Ikegami. Ikegami discloses a first ground line for maintaining a stable ground potential for an internal integrated circuit. The first ground line is connected to a second ground line disposed on a scribe region of the semiconductor chip via a bonding pad, which is connected to an external lead frame. In addition, an input/output circuit has a third ground line directly connected to the second ground line without passing the bonding pad.

Independent Claim 1 of the present Application, as amended, recites a substrate and a plurality of bond pads formed above the substrate. Also, Claim 1 recites a first isolated conductive trace formed at an outer region of the substrate and coupled to at least two of the plurality of bond pads. In contrast, Ikegami does not disclose a trace formed at an outer region of a substrate. Rather, the traces disclosed in Ikegami are used for operating the device, not for testing the device. In addition, Ikegami does not disclose a conductive trace that is isolated on the substrate. The trace in Ikegami is interconnected to other devices, which in turn are connected to lower device operating levels. For these reasons, Ikegami does not disclose all the elements of Claim 1. Independent Claim 10, as amended, recites elements analogous to those of Claim 1. Thus, Ikegami also does not disclose all the elements recited in Claim 10.

In conclusion, Ikegami does not disclose each and every element of the invention disclosed by independent Claims 1 and 10 and, as such, is not an anticipating reference of these claims. In addition, dependent Claims 2, 4-8, 11-12 and 14 depend from Claims 1 and 10, respectively. Thus, Ikegami is also not an anticipating reference for these dependent claims. Accordingly, the Applicants respectfully request the Examiner withdraw the §102 rejection with respect to Claims 1, 2, 4-8, 10-12 and 14.

## IV. Rejection of Claims 3 and 13 under 35 U.S.C. §103

The Examiner has rejected dependent Claims 3 and 13 under 35 U.S.C. §103(a) as being unpatentable over Ikegami, as applied above, in view of U.S. Patent No. 5,811,874 to Lee. The Applicants respectfully assert that the claimed invention is nonobvious in view of the combination of the foregoing references, and that the Examiner has not established a *prima facie* case of obviousness of dependent Claims 3 and 13.

As discussed above, Ikegami does not teach the isolated trace of the present invention, as recited in independent Claims 1 and 10. In addition, Ikegami does not suggest the use of an isolated trace since the conductive traces disclosed in Ikegami are not used for testing the integrity of internal circuitry. Also, there is no suggestion that the conductive traces of Ikegami be isolated, since they are used to provide power to the circuitry described therein. In addition, Lee merely provides for chamferred regions along conductive traces to reduce the shear stress of the traces. However, Lee does not teach or suggest the use of those conductive traces as isolated traces, but rather as part of the overall semiconductor chip device described therein. Therefore, since the combined teachings of Ikegami and Lee fails to teach or suggest all of the elements of the inventions of independent Claims 1 and 10, the combination does not establish a *prima facie* case of obviousness of dependent Claims 3 and 13, which include the elements of independent Claims 1 and 10, respectively. Accordingly, the Applicants respectfully request the Examiner withdraw the §103 rejection of dependent Claims 3 and 13.

In conclusion, Ikegami, whether viewed individually or in combination with Lee, fails to teach or suggest the invention recited in independent Claims 1 and 10 and their dependent claims, when considered as a whole. The Examiner has therefore not established a *prima facie* case of

obvious of Claims 3 and 13, and the Applicants respectfully request the Examiner withdraw the §103(a) rejection with respect to these claims.

## V. Conclusion

The Applicants respectfully request that the rejections be withdrawn and solicit a Notice of Allowance for Claims 1-8 and 10-14. The Applicants further attach hereto a marked-up version of the amendments made to the specification and the claims. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**".

Respectfully submitted,

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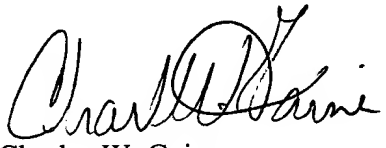

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## VERSION WITH MARKINGS TO SHOW CHANGES MADE



**IN THE CLAIMS:**

(1) Claim 1 has been amended as follows:

1. (Amended) An integrated circuit comprising:

a substrate;

a plurality of bond pads formed above the substrate; and

a first isolated conductive [region] trace formed at an outer region of the substrate and coupled to at least two of the plurality of bond pads.

(2) Claim 2 has been amended as follows:

2. (Amended) The integrated circuit of Claim 1 wherein the first isolated conductive [region] trace surrounds a plurality of bond pads.

(3) Claim 3 has been amended as follows:

3. (Amended) The integrated circuit of Claim 2 wherein the first isolated conductive [region] trace has a chamfered region.

(4) Claim 4 has been amended as follows:

4. (Amended) The integrated circuit of Claim 1 further comprising:

second conductive regions adapted to interconnect devices formed in the integrated circuit,

wherein the first isolated conductive [region] trace is separate from the devices.

(5) Claim 5 has been amended as follows:

5. (Amended) The integrated circuit of Claim 1 wherein the first isolated conductive [regions] trace comprises at least two separate first isolated conductive [regions] traces.

(6) Claim 6 has been amended as follows:

6. (Amended) The integrated circuit according to Claim 5 wherein the at least two separate first isolated conductive [regions] traces have a varying height relative to an upper surface of the substrate.

(7) Claim 7 has been amended as follows:

7. (Amended) The integrated circuit according to Claim 1 wherein the first isolated conductive [region] trace is formed at the periphery of the integrated circuit.

(8) Claim 8 has been amended as follows:

8. (Amended) The integrated circuit of Claim 1 wherein the first isolated conductive [region] trace comprises at least two separate isolated conductive [regions] traces, each of the separate isolated conductive [regions] traces coupled to at least two of the plurality of bond pads.

(9) Claim 9 has been canceled without prejudice or disclaimer.

(10) Claim 10 has been amended as follows:

10. (Amended) An integrated circuit comprising:

a substrate;

a plurality of bond pads; and

[a] an isolated conductive tester runner formed on the substrate and around the plurality of bond pads, the isolated conductive tester runner electrically coupled to at least two of the plurality of bond pads.

(11) Claim 11 has been amended as follows:

11. (Amended) The integrated circuit of Claim 10 further comprising a plurality of [the] isolated conductive tester runners.

(12) Claim 12 has been amended as follows:

12. (Amended) The integrated circuit according to Claim 11 wherein at least two of the plurality of the isolated conductive tester runners having a varying height relative to an upper surface of the substrate.

(13) Claim 13 has been amended as follows:

13. (Amended) The integrated circuit of Claim 10 wherein the isolated conductive tester runner has a chamfered region.

(14) Claim 14 has been amended as follows:

14. (Amended) The integrated circuit of Claim 10 further comprising:

devices formed on the integrated circuit; and

circuit conductive runners adapted to interconnect the devices to form a circuit;

wherein the isolated conductive [runners are] tester runner formed on the substrate and around the plurality of bond pads is separate from the devices.

(15) Claim 15 has been amended without prejudice or disclaimer.